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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/764,484	01/27/2004	Atsuhiko Mori	61282-059	6279

7590 04/19/2006

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EXAMINER

MASDON, DAVID T

ART UNIT PAPER NUMBER

2188

DATE MAILED: 04/19/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary

Application No.

10/764,484

Applicant(s)

MORI, ATSUIHIRO

Examiner

David Masdon

Art Unit

2188

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 05 August 2004.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-7 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-7 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 05 August 2004 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☒ All b) ☐ Some * c) ☐ None of:
1. ☒ Certified copies of the priority documents have been received.
2. ☐ Certified copies of the priority documents have been received in Application No. _____.
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- 1) ☒ Notice of References Cited (PTO-892)
- 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
- 3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08)
Paper No(s)/Mail Date 1/27/04 & 8/5/04.
- 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____.
- 5) ☐ Notice of Informal Patent Application (PTO-152)
- 6) ☐ Other: _____.

DETAILED ACTION

Information Disclosure Statement

1. The information disclosure statements (IDS) were submitted on 1/27/2004 & 8/5/2004. The submissions are in compliance with the provisions of 37 CFR 1.97. Accordingly, the information disclosure statements are being considered by the examiner.

Drawings

2. The drawings filed on 8-5-2004 have been approved by the examiner.

Claim Rejections - 35 USC § 102

3. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

4. Claims 1-7 rejected under 35 U.S.C. 102(b) as being anticipated by Larson. (US 6,292,807)

With regard to claim 1, Larson discloses an information processing apparatus comprising:

data storing means; [(memory) column 2, line 42]

first and second data input/output means for giving access to the data storing means; [(plurality of I/O interfaces) column 4, lines 6-7]

clock generating means for supplying a clock to the second data input/output means; [(access request referenced to clock signal) column 4, line 41]

switching means for switching access of the first data input/output means and the second data input/output means to the data storing means; and [(selection circuit) column 7, line 65]

access arranging means for causing the clock for the second data input/output means to wait and executing the access of the first data input/output means earlier when a contention of the access of the first data input/output means and the second data input/output means to the data storing means is generated, [(request queue that produces age signal) column 4, lines 61-63]

and for starting the access of the second data input/output means after the access of the first data input/output means is ended. [(selectively shift entries in request queue) column 5, line 3]

With regard to claim 2, Larson discloses an information processing apparatus comprising:

a built-in memory; [(memory is coupled to processor; cache controller) column 3, line 42-48]

a processor for processing data stored in the built-in memory; [(central processing unit) column 3, line 30]

clock generating means for supplying a clock signal to the processor; [(access request referenced to clock signal) column 4, line 41]

input/output control means for executing access to the built-in memory upon receipt of an instruction from an external control device; and [(request ordering circuitry receives age signals and controls operations of the request transmission circuitry) column 4, lines 64-67]

access arranging means for generating a wait request signal to cause the clock signal to wait and carrying out access of the input/output control means with a priority when a contention of access of the processor and the input/output control means to the built-in memory is generated. [(request queue that produces age signal) column 4, lines 61-63]

With regard to claim 3, Larson discloses the information processing apparatus according to claim 2, further comprising selecting means for switching the access the processor and the input/output control means to the built-in memory,

wherein the access arranging means outputs a control signal to the selecting means when a request for the access of the input/output control means to the built-in memory is generated during the access of the processor to the built-in memory, [(request queue that produces age signal) column 4, lines 61-63]

and the selecting means receiving the control signal switches the access of the processor to the access of the input/output control means to the built-in memory.

[(selectively shift entries in request queue) column 5, line 3]

With regard to claim 4, Larson discloses the information processing apparatus according to claim 2, further comprising holding means for holding read data output from the built-in memory before a wait operation of the processor during the wait operation of the processor, [(holding stored values) column 7, line 54]

wherein the access arranging means switches read data to be supplied to the processor between the read data output from the built-in memory and the read data held by the holding means. [(selecting which signal path applied to input) column 7, lines 66-67] Larson discloses selecting which memory will supply the processor. The applicant discloses two different types of read data: built-in memory and holding means. Larson discloses both these types of read data. Therefore, the invention that the applicant discloses is analogous to what Larson discloses.

With regard to claim 5, Larson discloses a memory access arranging method of an information processing apparatus including data storing means and first and second data input/output means for giving access to the data storing means, comprising the steps of:

causing a clock for the second data input/output means to wait when a contention of the access of the first data input/output means and the second data input/output means to the data storing means is generated; [(request queue that produces age signal) column 4, lines 61-63]

executing the access of the first data input/output means earlier; and [(selecting which signal path applied to input) column 7, lines 66-67]

canceling the clock wait of the second data input/output of the first data input/output means after ending the access means, and executing the access of the second data input/output means. [(memory access requests referenced to clock signal) column 4, lines 40-41] Larson discloses basing the memory access requests off of a clock. This is analogous to applicant utilizing a "clock wait" as a reference for ending and executing memory access.

With regard to claim 6, Larson discloses a memory access arranging method of an information processing apparatus including a processor for carrying out a pipeline processing over an instruction, [(pipelined memory) column 3, line 20] a memory provided in the processor, [(memory is coupled to processor; cache controller) column 3, line 42-48] and input/output control means for executing access to the memory with a higher priority than the processor, [(request queues) column 2, line 44] comprising the steps of:

generating a wait request signal for causing supplied to the processor to wait when a contention clock of access of the processor and the input/output control means to the memory is generated; [(request queue that produces age signal) column 4, lines 61-63]

switching the access of the processor to the access of the input/output control means to the memory; and [(selection circuit) column 7, line 65]

canceling the clock wait of the processor after ending the access of the input/output control means to the memory, and executing the access of the processor to

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the memory. [(memory access requests referenced to clock signal) column 4, lines 40-41]

Larson discloses basing the memory access requests off of a clock. This is analogous to applicant utilizing a "clock wait" as a reference for ending and executing memory access.

Claim 7 rejected with same rationale as claim 4 & 5.

Conclusion

5. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Roy	6,125,421
Mattausch	6,557,085
Vander Mey	4,096,571
Holtey	4,271,467
Moore	3,603,935
Kato et al	6,480,904
Khare et al	6,487,643
Dyer	6,629,220
Joffe et al	6,205,523
Barnaby et al	6,006,303

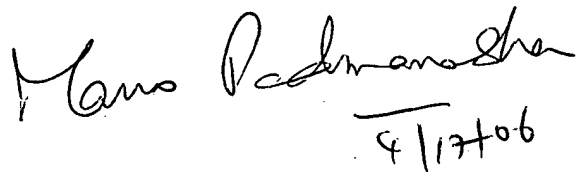
6. Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Masdon whose telephone number is (571)272-6815. The examiner can normally be reached on Monday - Friday, 7am - 4:30pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Mano Padmanabhan can be reached on (571)272-4210. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

DM

Thursday, April 13, 2006



Handwritten signature of Mano Padmanabhan, dated 4/13/06.

MANO PADMANABHAN
SUPERVISORY PATENT EXAMINER